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Takayuki MATSUZUKA	:	Confirmation Number: 4957
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For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

VERIFICATION OF ENGLISH TRANSLATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I, Kazumasa YAMADA, declare that I am conversant in both the Japanese and English languages and that the English translation as attached hereto is an accurate translation of Japanese Patent Application No. 2003-14645 filed on January 23, 2003, 2001.

Signed this 24th day of February, 2006

Kazumasa Yamada
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Item: Specification 1 copy
Item: Drawing 1 copy
Item: Abstract 1 copy

Request for proof transmission: Yes

[Document Name]

Specification

[Title of the Invention]

Semiconductor Integrated Circuit Device

[Claims]

[Claim 1] A semiconductor integrated circuit device comprising:

a resonant circuit which makes resonance at an arbitrary frequency;

a transmission line for transmitting a high-frequency signal having said frequency, one of two end portions of said transmission line being connected to said resonant circuit;

an active element having a first electrode connected to the other end portion of said transmission line, a second electrode which is grounded through a reactance element, and a third electrode;

an output-matching circuit including a diode section for regulating an oscillation power and a high-frequency signal output terminal, one of two end portions of said diode section being connected to said third electrode of said active element, and said high-frequency signal output terminal being connected to the other end portion of said diode section; and

a substrate having a main surface on which said resonant circuit, said transmission line, said active element and said output-matching circuit are arranged.

[Claim 2] The semiconductor integrated circuit device according to claim 1, wherein said diode section includes a plurality of diodes arranged in an inverse parallel manner.

[Claim 3] The semiconductor integrated circuit device according to claim 1, wherein said diode section includes a plurality of diodes arranged in series.

[Claim 4] The semiconductor integrated circuit device according to claim 1, further comprising a bias circuit for applying a DC bias to said diode section.

[Claim 5] A semiconductor integrated circuit device comprising:

- a resonant circuit which makes resonance at an arbitrary frequency;

- a transmission line for transmitting a high-frequency signal having said frequency, one of two end portions of said transmission line being connected to said resonant circuit;

- an oscillation power regulating circuit including a diode section for regulating an oscillation power, one end portion of said oscillation power regulating circuit being connected to the other end portion of said transmission line;

- an active element having a first electrode connected to

the other end portion of said transmission line, a second electrode which is grounded through a reactance element, and a third electrode;

an output-matching circuit including a high-frequency signal output terminal, said output-matching circuit being connected to said third electrode of said active element; and

a substrate having a main surface on which said resonant circuit, said transmission line, said oscillation power regulating circuit, said active element and said output-matching circuit are arranged.

[Claim 6] The semiconductor integrated circuit device according to claim 5, wherein said diode section includes a plurality of diodes arranged in an inverse parallel manner.

[Claim 7] The semiconductor integrated circuit device according to claim 5, wherein said diode section includes a plurality of diodes arranged in series.

[Claim 8] The semiconductor integrated circuit device according to claim 5, further comprising a bias circuit for applying a DC bias to said diode section.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to a semiconductor

integrated circuit device, more particularly to an oscillator which is principally operated in a microwave or millimetric-wave region.

[0002]

[Prior Art]

An oscillator composed of a semiconductor integrated circuit is well known. In the oscillator, on a substrate, there are provided a resonant circuit for generating a high-frequency signal having a predetermined frequency, and a transistor for amplifying the high-frequency signal (For example, see Patent Document 1.).

[0003]

Meanwhile, in the conventional oscillator of this type, it is probable that an excessive power is inputted to the transistor in an equilibrium state of oscillation so that the device breakdown or deterioration of noise characteristic is caused. Therefore, in the conventional oscillator, in general, in order to avoid these disadvantages, the small signal loop gain is decreased to achieve the equilibrium state of oscillation by a lower electric power.

[0004]

[Patent Document 1]

Japanese Laid-open Patent Publication No. 64-5206
(Left-Lower Column and Right-lower column in Page 2, Fig. 1)

[0005]

[Problems that the Invention is to solve]

As described above, in the conventional oscillator, in order to reduce the power inputted to the transistor in the equilibrium state of oscillation, the small signal loop gain is decreased to achieve the equilibrium state of oscillation by a lower power. In consequence, in the conventional oscillator, for example, the variation in characteristic to the variation in gain of the transistor is increased due to the variations in the environment temperature or manufacturing condition or the like. Thus, there occurs such a problem that a countermeasure for an excessive input of the power cannot be actually achieved in many cases.

[0006]

The present invention, which has been developed to solve the conventional problems described above, has an object or a problem to be solved to provide a semiconductor integrated circuit device or an oscillator which can decrease an oscillation power when an equilibrium state of oscillation is achieved, without decreasing a small signal loop gain.

[0007]

[Means for solving the Problems]

A semiconductor integrated circuit device according to the present invention, which has been achieved to solve the

above-mentioned problems, is characterized in that it has a circuit structure for regulating the power amplitude by using a diode. More specifically, in the semiconductor integrated circuit device, a resonant circuit, a transmission line, an active element and an output-matching circuit are arranged on one main surface (or a spreading surface) of a substrate. The resonant circuit resonates at an arbitrary (or predetermined) frequency. The transmission line has an end portion connected to the resonant circuit and transmits a high-frequency signal of the frequency. The active element has a first electrode connected to the other end portion of the transmission line, a second electrode which is grounded through a reactance element, and a third electrode. The output-matching circuit includes a diode section for regulating an oscillation power and a high-frequency signal output terminal. An end portion of the diode section is connected to the third electrode of the active element. The high-frequency signal output terminal is connected to the other end portion of the diode section.

[0008]

[Embodiments]

Several embodiments of the present invention will be described below with reference to the accompanying drawings.

[0009]

(First Embodiment)

With reference to Figs. 1 to 3, the first embodiment of the present invention will be described below. Fig. 1 shows the oscillator according to the first embodiment of the present invention. Fig. 2 shows the relationship between the reflection characteristic of a diode and the oscillation power in the oscillator shown in Fig. 1. Fig. 3 shows the relationship between the loop gain and the oscillation power in the oscillator shown in Fig. 1.

[0010]

As shown in Fig. 1, in the oscillator (semiconductor integrated circuit device) according to the first embodiment, a FET 1 (field effect transistor), an output-matching circuit C2 having a diode 2 and an output terminal 10, an LC series resonant circuit C1 having a capacitor 3 and an inductor 4, a transmission line 5, and a source inductor 6 are arranged on one main surface (spreading surface) of a substrate (not shown) composed of a semiconductor material.

[0011]

The capacitor 3 and the inductor 4 constituting the LC series resonant circuit C1 are connected in series with each other. One counter electrode of the capacitor 3 is grounded, while the other counter electrode is connected to one end of the inductor 4. The other end of the inductor 4 is connected to one end of the transmission line 5. In this manner, when

oscillating electric signals are supplied from the outside to the LC series resonant circuit C1, the LC series resonant circuit C1 resonates at a predetermined frequency (resonant frequency) to generate a high-frequency signal having the resonant frequency, and outputs the high-frequency signal to the transmission line 5. A variable capacitor (e.g. a varactor diode) may be used in place of the capacitor 3. In this case, when the capacitance of the variable capacitor is changed, the oscillation frequency can be changed.

[0012]

The other end of the transmission line 5 is connected to the gate (first electrode) of the FET 1. In consequence, the transmission line 5 transmits the high-frequency signal having the resonant frequency, which is inputted from the LC series resonant circuit C1, to the gate of the FET 1. In this case, the transmission line 5 determines the phase condition of the high-frequency signal.

[0013]

The source (second electrode) of the FET 1 is grounded through the source inductor 6 (reactance element). The drain (third electrode) of the FET 1 is connected to the anode of the diode 2 constituting the output-matching circuit C2. The FET 1 amplifies the high-frequency signal inputted into the gate, and outputs the high-frequency signal from the drain to the

output-matching circuit C2 (diode 2). The diode 2 regulates the oscillation power. The cathode of the diode 2 is connected to the output terminal 10 for outputting the high-frequency signal to the outside.

[0014]

As described above, in the oscillator according to the first embodiment, the FET 1 is used as an active element. However, any active element of another type, e.g. a bipolar transistor may be used in place of the FET 1. In Fig. 1, the bias circuit of the FET 1 is omitted to simplify the drawing. The same applies to the following second to eighth embodiments 2.

[0015]

In the oscillator shown in Fig. 1, the diode 2 is arranged to have a forward direction from the FET 1 to the output terminal 10. However, the diode 2 may be arranged to have a reverse direction opposing the direction shown in Fig. 1. The circuits described above may be integrally formed on the semiconductor substrate like, e.g. an MMIC (Monolithic Microwave Integrated Circuit). In addition, the circuit parts may be mounted after a transmission line pattern is formed on a ceramic substrate or the like.

[0016]

In the oscillator according to the first embodiment, as the oscillation power increases with growth of oscillation, the

amplitude of the voltage applied across both the ends of the diode 2 increases. When the forward voltage applied to the diode 2 exceeds a threshold voltage, the impedance of the diode 2 decreases. In this case, as shown in Fig. 2, the rate of the power reflected by the diode 2 decreases. As the result, as shown in Fig. 3, the loop gain in the entire circuit decreases. Therefore, the oscillation power obtained when the equilibrium state of oscillation is achieved, can be made smaller than that of a conventional oscillator without decreasing the small-signal loop gain.

[0017]

(Second Embodiment)

The second embodiment of the present invention will be described below with reference to Figs. 4 and 5. However, the oscillator according to the second embodiment and the oscillator according to the first embodiment shown in Fig. 1 have a lot in common. Therefore, different points between the oscillator according to the second embodiment and the oscillator according to the first embodiment will be mainly described below to avoid overlapped descriptions.

[0018]

Fig. 4 shows the oscillator according to the second embodiment. Fig. 5 shows the relationship between the loop gain and the oscillation power in the oscillator shown in Fig. 4.

As shown in Fig. 4, in the oscillator according to the second embodiment, the output-matching circuit C2 is provided with two diodes 2a and 2b which are arranged and connected in an inverse parallel manner. The other points are equal to those of the oscillator according to the first embodiment.

[0019]

In the oscillator according to the second embodiment, since the two diodes 2a and 2b are arranged in the inverse parallel manner, the same effect as that of the oscillator according to the first embodiment can be obtained on both the positive potential side and the negative potential side regarding to the amplitude of the oscillation power. In the oscillator according to the first embodiment, the effect can be obtained on only one side because only one diode 2 is arranged. In this manner, as shown in Fig. 5, in the oscillator according to the second embodiment, the oscillation power obtained when the equilibrium state of oscillation is achieved, can be made smaller than that in the first embodiment without decreasing the small-signal loop gain.

[0020]

(Third Embodiment)

The third embodiment of the present invention will be described below with reference to Figs. 6 and 7. Since the oscillator according to the third embodiment and the oscillator

according to the first embodiment shown in Fig. 1 have a lot in common, different points between the oscillator according to the third embodiment and the oscillator according to the first embodiment will be mainly described below.

[0021]

Fig. 6 shows the oscillator according to the third embodiment. Fig. 7 shows the relationship between the loop gain and the oscillation power in the oscillator shown in Fig. 6. As shown in Fig. 6, in the oscillator according to the third embodiment, the output-matching circuit C2 is provided with two diodes 2c and 2d which are arranged or connected in series with each other in the same direction. The other points are equal to those of the oscillator according to the first embodiment. The two diodes 2c and 2d may be arranged in the direction opposing the direction in Fig. 6.

[0022]

In the oscillator according to the third embodiment, since the two diodes 2c and 2d are arranged in series with each other in the same direction, voltages applied to the diodes 2c and 2d are lower than those in the first embodiment. In consequence, as shown in Fig. 7, the oscillation power obtained when the equilibrium state of oscillation is achieved, can be made larger than that in the first embodiment in the range smaller than that of a conventional oscillator without decreasing the small-signal

loop gain.

[0023]

(Fourth Embodiment)

The fourth embodiment of the present invention will be described below with reference to Figs. 8 and 9. Since the oscillator according to the fourth embodiment and the oscillator according to the first embodiment shown in Fig. 1 have a lot in common, different points between the oscillator according to the fourth embodiment and the oscillator according to the first embodiment will be mainly described below.

[0024]

Fig. 8 shows the oscillator according to the fourth embodiment. Fig. 9 shows the relationship between the loop gain and the oscillation power in the oscillator shown in Fig. 8. As shown in Fig. 8, in the oscillator according to the fourth embodiment, two choke inductors 7a and 7b (bias circuits) for applying DC biases to the diode 2 are arranged at portions on the anode and cathode sides of the diode 2, respectively. In addition, the output-matching circuit C2 is provided with a DC blocking capacitor 8. The other points are the same as those in the oscillator according to the first embodiment. The diode 2 may be arranged in the direction opposing the direction of the diode 2 in Fig. 8.

[0025]

In the oscillator according to the fourth embodiment, since the DC biases can be applied to the diode 2, the center voltage of the amplitude of the high-frequency voltage applied to the diode 2 can be set to an arbitrary voltage. In consequence, as shown in Fig. 9, the oscillation power obtained when the equilibrium state of oscillation is achieved, can be made equal to an arbitrary value in the range smaller than that of a conventional oscillator without decreasing the small-signal loop gain.

[0026]

(Fifth Embodiment)

The fifth embodiment of the present invention will be described below with reference to Figs. 10 to 12. Since the oscillator according to the fifth embodiment and the oscillator according to the first embodiment shown in Fig. 1 have a lot in common, different points between the oscillator according to the fifth embodiment and the oscillator according to the first embodiment will be mainly described below.

[0027]

Fig. 10 shows the oscillator according to the fifth embodiment. Fig. 11 shows the relationship between the pass characteristic of the oscillation power regulating circuit using a diode and the oscillation power in the oscillator shown in Fig. 10. Fig. 12 shows the relationship between the loop gain

and the oscillation power in the oscillator shown in Fig. 10.

[0028]

As shown in Fig. 10, in the oscillator according to the fifth embodiment, an amplitude power regulating circuit 9 for regulating the oscillation power by using the diode 2 is arranged at a portion between the transmission line 5 and the FET 1. The anode of the diode 2 is connected to the line between the transmission line 5 and the gate of the FET 1, and the cathode of the diode 2 is grounded. In this oscillator, any diode for regulating an oscillation power is not arranged in the output-matching circuit C2. The other points are equal to those in the oscillator according to the first embodiment. The diode 2 may be arranged in the direction opposing the direction of the diode 2 in Fig. 10.

[0029]

In the oscillator according to the fifth embodiment, as the oscillation power increases with growth of oscillation, the amplitude of the power applied across both the ends of the diode 2 increases. When a forward voltage applied to the diode 2 exceeds a threshold voltage, the impedance of the diode 2 decreases. In this case, as shown in Fig. 11, the rate of the power passing through the amplitude power regulating circuit 9 decreases. As the result, as shown in Fig. 12, the loop gain in the entire circuit decreases. Therefore, the oscillation

power obtained when the equilibrium state of oscillation is achieved, can be made smaller than that of a conventional oscillator without decreasing the small-signal loop gain.

[0030]

(Sixth Embodiment)

The sixth embodiment of the present invention will be described below with reference to Figs. 13 and 14. However, the oscillator according to the sixth embodiment and the oscillator according to the fifth embodiment shown in Fig. 10 have a lot in common. Therefore, different points between the oscillator according to the sixth embodiment and the oscillator according to the fifth embodiment will be mainly described below to avoid overlapped descriptions.

[0031]

Fig. 13 shows the oscillator according to the sixth embodiment. Fig. 14 shows the relationship between the loop gain and the oscillation power in the oscillator shown in Fig. 13. As shown in Fig. 13, in the oscillator according to the sixth embodiment, the amplitude power regulating circuit 9 is provided with two diodes 2e and 2f which are arranged or connected in an inverse parallel manner. The other points are equal to those of the oscillator according to the fifth embodiment.

[0032]

In the oscillator according to the sixth embodiment, since

the two diodes 2e and 2f are arranged in the inverse parallel manner in the amplitude power regulating circuit 9, the same effect as that of the oscillator according to the fifth embodiment can be obtained on both the positive potential side and the negative potential side, regarding to the amplitude of the oscillation power. In consequence, as shown in Fig. 14, the oscillation power obtained when the equilibrium state of oscillation is achieved, can be made smaller than that in the fifth embodiment in the range smaller than that of a conventional oscillator without decreasing the small-signal loop gain.

[0033]

(Seventh Embodiment)

The seventh embodiment of the present invention will be described below with reference to Figs. 15 and 16. Since the oscillator according to the seventh embodiment and the oscillator according to the fifth embodiment shown in Fig. 10 have a lot in common, different points between the oscillator according to the seventh embodiment and the oscillator according to the fifth embodiment will be mainly described below.

[0034]

Fig. 15 shows the oscillator according to the seventh embodiment. Fig. 16 shows the relationship between the loop gain and the oscillation power in the oscillator shown in Fig. 15. As shown in Fig. 15, in the oscillator according to the

seventh embodiment, the amplitude power regulating circuit 9 is provided with two diodes 2g and 2h which are arranged or connected in series with each other in the same direction. The other points are equal to those in the oscillator according to the fifth embodiment. The diodes 2g and 2h may be arranged in the direction opposing the direction in Fig. 15.

[0035]

In the oscillator according to the seventh embodiment, since the two diodes 2g and 2h are arranged in series with each other in the same direction in the amplitude power regulating circuit 9, voltages applied to the diodes 2g and 2h are lower than those of the fifth embodiment. In consequence, as shown in Fig. 16, the oscillation power obtained when the equilibrium state of oscillation is achieved, can be made larger than that in the fifth embodiment in the range smaller than that of a conventional oscillator without decreasing the small-signal loop gain.

[0036]

(Eighth Embodiment)

The eighth embodiment of the present invention will be described below with reference to Figs. 17 and 18. Since the oscillator according to the eighth embodiment and the oscillator according to the fifth embodiment shown in Fig. 10 have a lot in common, different points between the oscillator according

to the eighth embodiment and the oscillator according to the fifth embodiment will be mainly described below.

[0037]

Fig. 17 shows the oscillator according to the eighth embodiment. Fig. 18 shows the relationship between the loop gain and the oscillation power in the oscillator shown in Fig. 17. As shown in Fig. 17, in the oscillator according to the eighth embodiment, a choke inductor 7 for applying DC biases to the diode 2 is connected to the line between the transmission line 5 and the amplitude power regulating circuit 9. The other points are the same as those in the oscillator according to the fifth embodiment. The diode 2 may be arranged in the direction opposing the direction of the diode 2 in Fig. 17.

[0038]

In the oscillator according to the eighth embodiment, since the DC biases can be applied to the diode 2, the center voltage of the amplitude of the high-frequency voltage applied to the diode 2 can be set to an arbitrary voltage. In consequence, as shown in Fig. 18, the oscillation power obtained when the equilibrium state of oscillation is achieved, can be made equal to an arbitrary value in the range smaller than that of a conventional oscillator without decreasing the small-signal loop gain.

[0039]

[Advantages of the Invention]

As described above, the semiconductor integrated circuit device according to the present invention has the circuit structure which regulates the power amplitude by using the diode. In consequence, the oscillation power obtained when the equilibrium state of oscillation is achieved, can be decreased without decreasing the small signal loop gain.

[Brief Description of the Drawings]

[Fig. 1] This is a circuit diagram of an oscillator according to the first embodiment of the present invention.

[Fig. 2] This is a graph showing a relationship between a reflection characteristic of a diode and an oscillation power in the oscillator shown in Fig. 1.

[Fig. 3] This is a graph showing a relationship between a loop gain and an oscillation power in the oscillator shown in Fig. 1.

[Fig. 4] This is a circuit diagram of an oscillator according to the second embodiment of the present invention.

[Fig. 5] This is a graph showing a relationship between a loop gain and an oscillation power in the oscillator shown in Fig. 4.

[Fig. 6] This is a circuit diagram of an oscillator according to the third embodiment of the present invention.

[Fig. 7] This is a graph showing a relationship between a loop gain and an oscillation power in the oscillator shown in Fig. 6.

[Fig. 8] This is a circuit diagram of an oscillator according to the fourth embodiment of the present invention.

[Fig. 9] This is a graph showing a relationship between a loop gain and an oscillation power in the oscillator shown in Fig. 8.

[Fig. 10] This is a circuit diagram of an oscillator according to the fifth embodiment of the present invention.

[Fig. 11] This is a graph showing a relationship between a pass characteristic of an oscillation power regulating circuit and an oscillation power in the oscillator shown in Fig. 10.

[Fig. 12] This is a graph showing a relationship between a loop gain and an oscillation power in the oscillator shown in Fig. 10.

[Fig. 13] This is a circuit diagram of an oscillator according to the sixth embodiment.

[Fig. 14] This is a graph showing a relationship between a loop gain and an oscillation power in the oscillator shown in Fig. 13.

[Fig. 15] This is a circuit diagram of an oscillator according to the seventh embodiment.

[Fig. 16] This is a graph showing a relationship between

a loop gain and an oscillation power in the oscillator shown in Fig. 15.

[Fig. 17] This is a circuit diagram of an oscillator according to the eighth embodiment of the present invention.

[Fig. 18] This is a graph showing a relationship between a loop gain and an oscillation power in the oscillator shown in Fig. 17.

[Explanation of Reference Numerals and Signs]

- C1: LC series resonant circuit
- C2: Output matching circuit
- 1: FET
- 2: Diode
- 2a-2h: Diodes
- 3: Capacitor
- 4: Inductor
- 5: Transmission line
- 6: Source inductor
- 7: Choke inductor
- 7a: Choke inductor
- 7b: Choke inductor
- 8: DC blocking capacitor
- 9: Amplitude power regulating circuit
- 10: Output terminal

[Document Name] Abstract

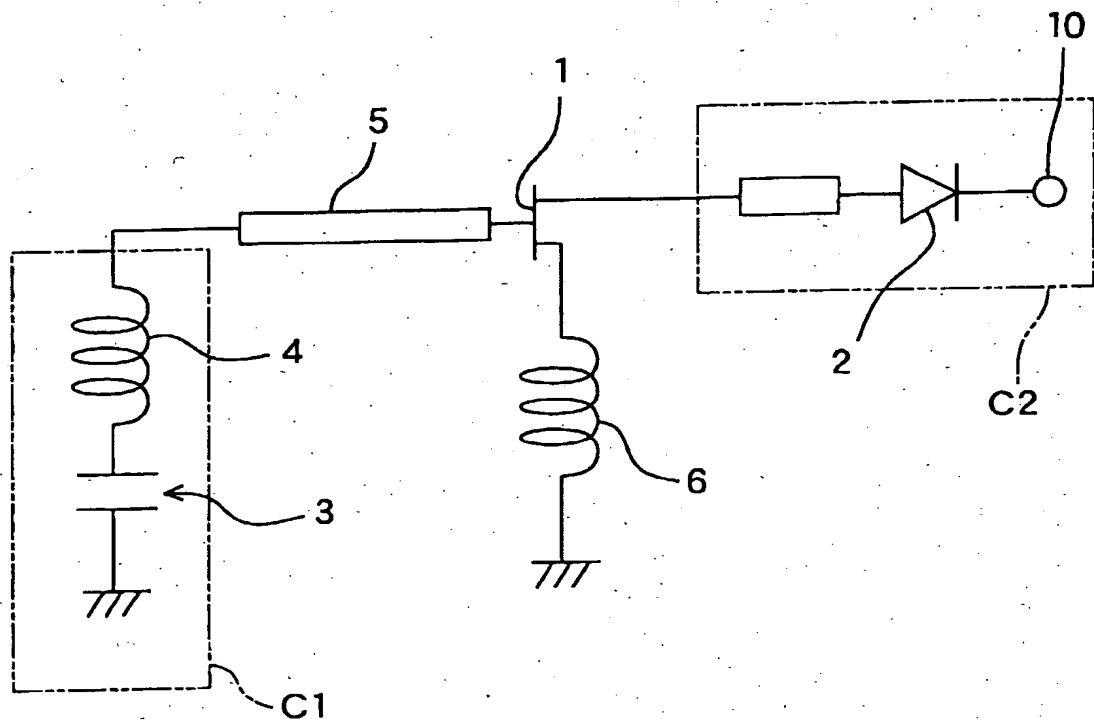
[Abstract]

[Problem] To provide an oscillator which can decrease an oscillation power when an equilibrium state of oscillation is achieved, without decreasing a small signal loop gain.

[Solution] In an oscillator, on one major surface of a substrate consisting of a semiconductor material there are arranged a FET 1, an output matching circuit C2 having a diode 2, an LC series resonant circuit C1 having a capacitor 3 and an inductor 4, a transmission line 5, and a source inductor 6. The source of the FET 1 is grounded through a source inductor 6. The drain of the FET 1 is connected to the anode of the diode 2 constituting an output matching circuit C2 through a transmission line 10. The FET 1 amplifies a high-frequency signal input to the gate, and outputs the high-frequency signal from the drain to an output matching circuit C2. The diode 2 regulates an oscillation power.

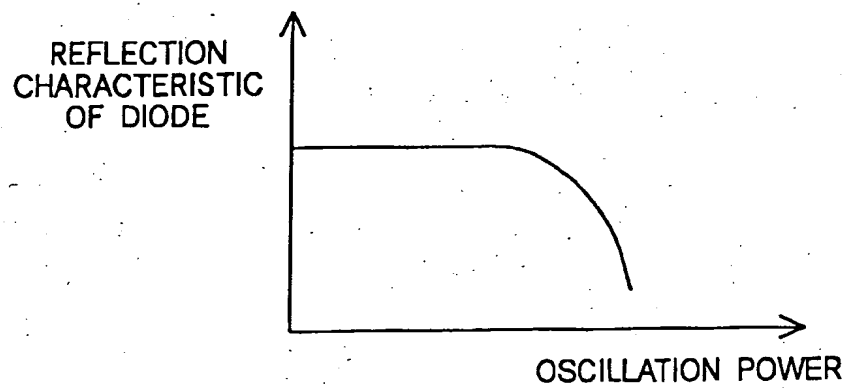
[Selected Drawing] Fig. 1

[Fig. 1]

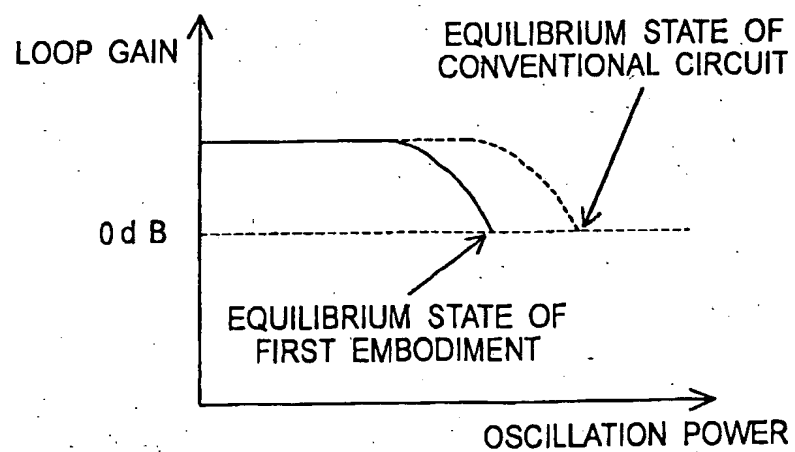


- 1: FET
- 2: Diode
- 3: Capacitor
- 4: Inductor
- 5: Transmission line
- 6: Source inductor
- C1: LC series resonant circuit
- C2: Output matching circuit

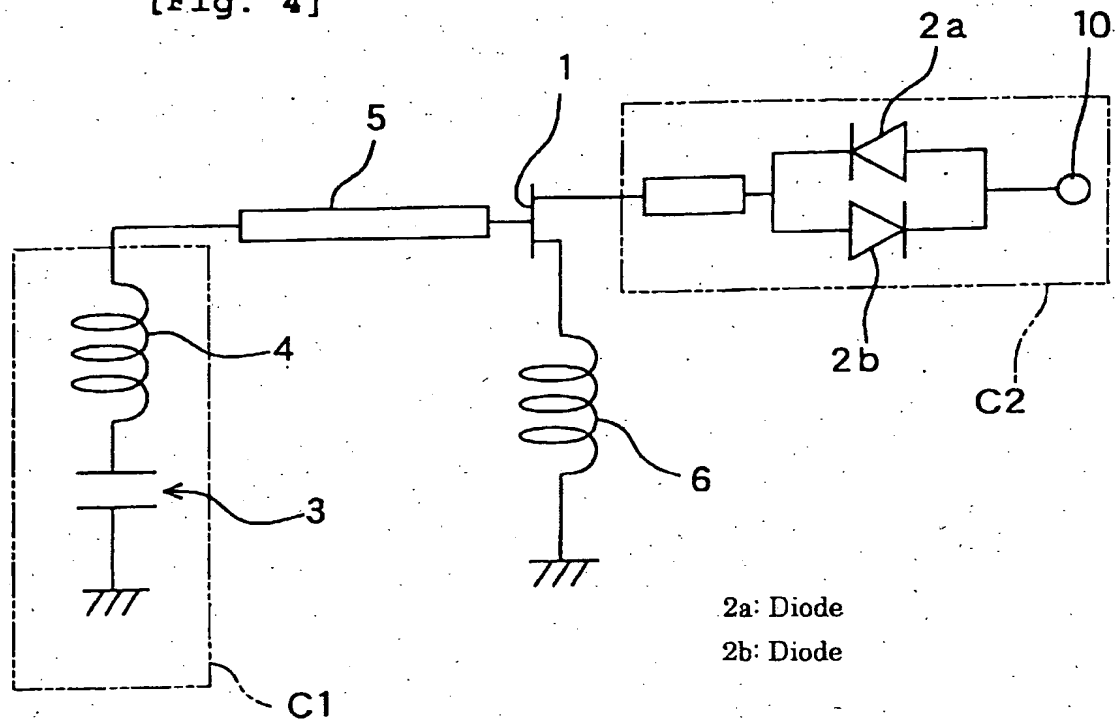
[Fig. 2]



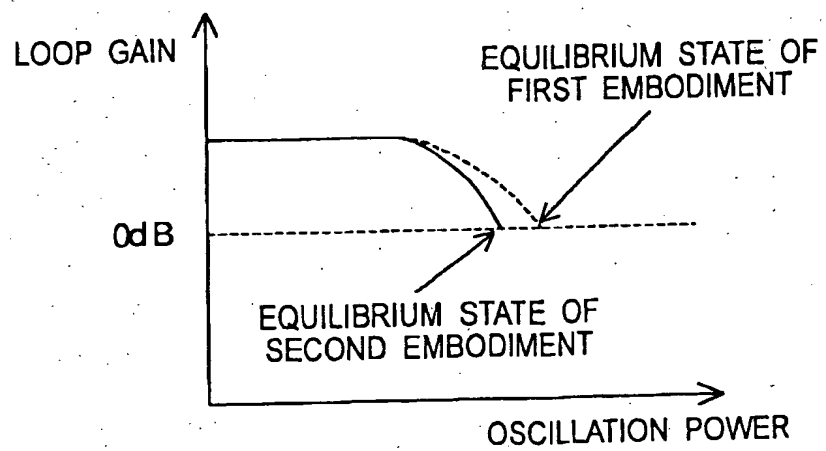
[Fig. 3]



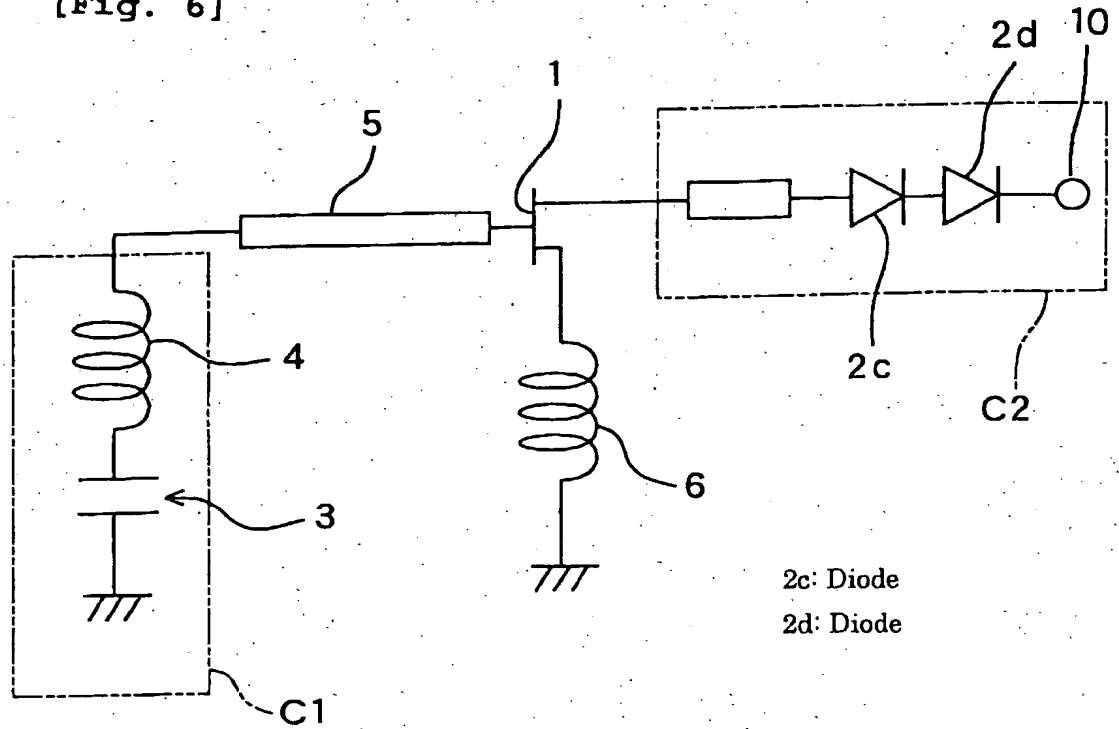
[Fig. 4]



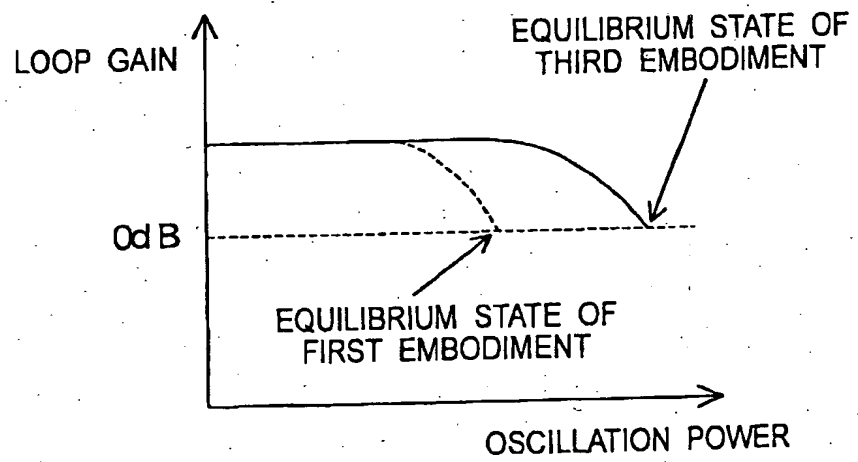
[Fig. 5]



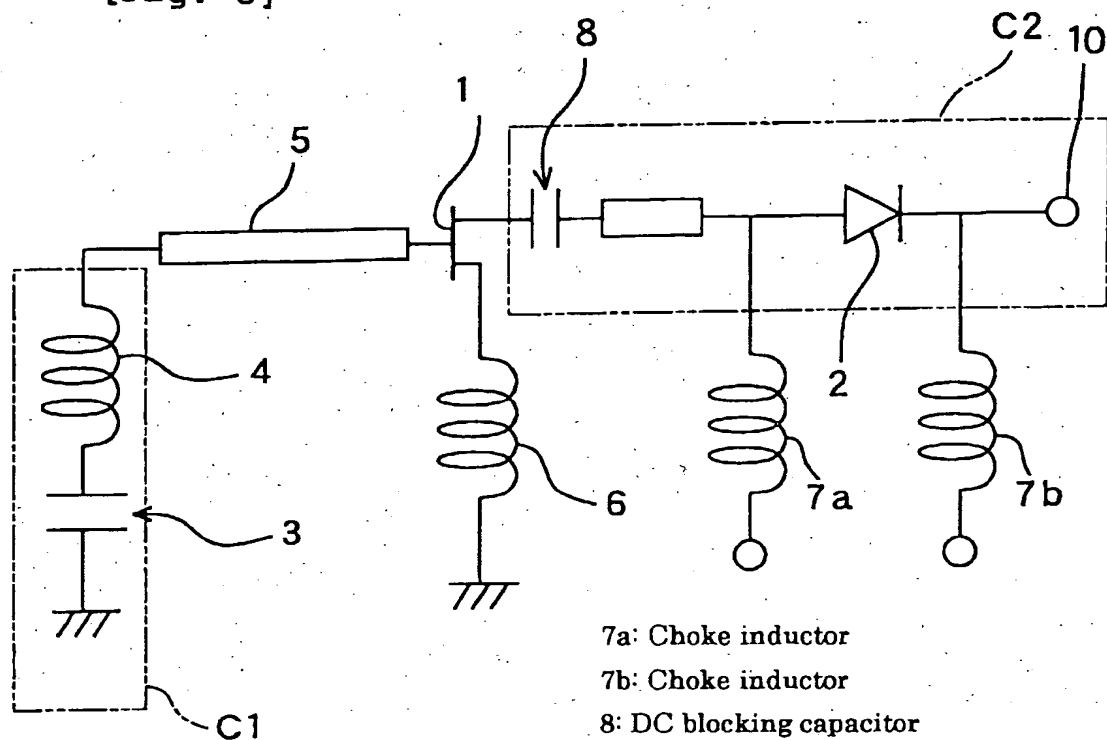
[Fig. 6]



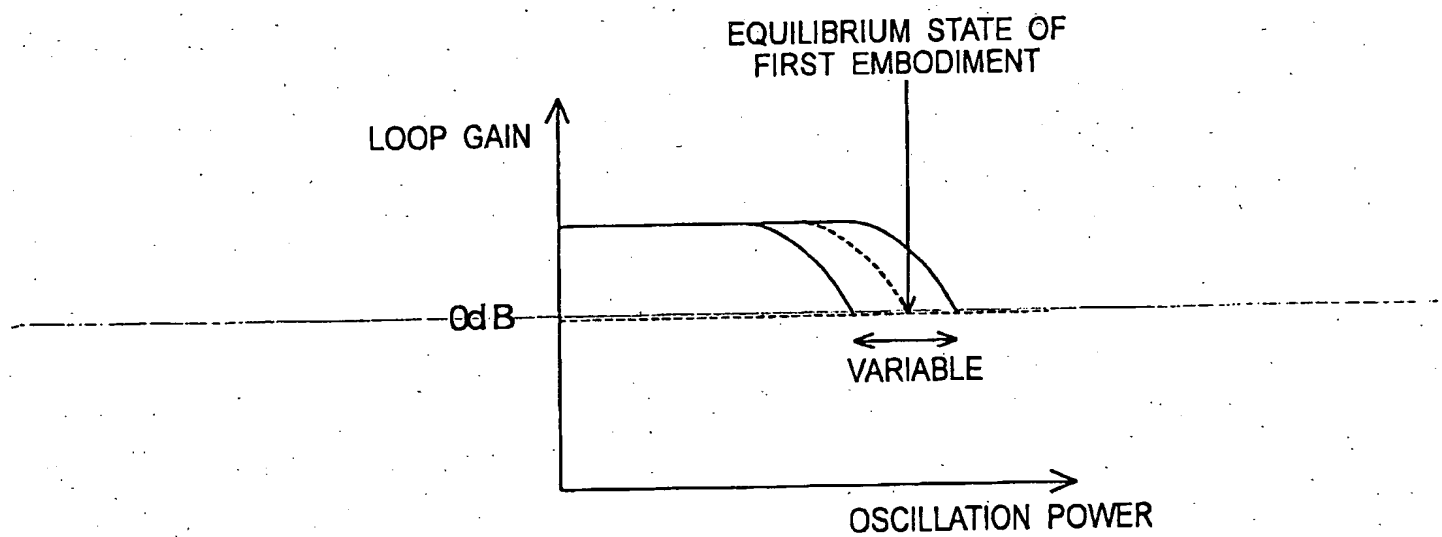
[Fig. 7]



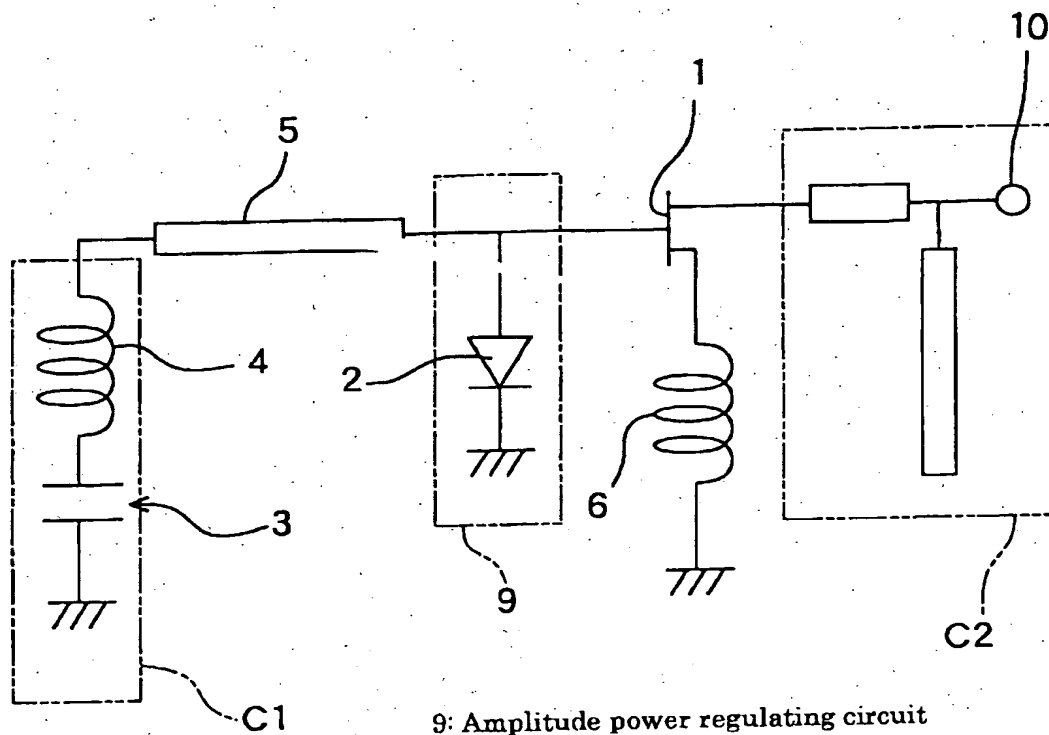
[Fig. 8]



[Fig. 9]

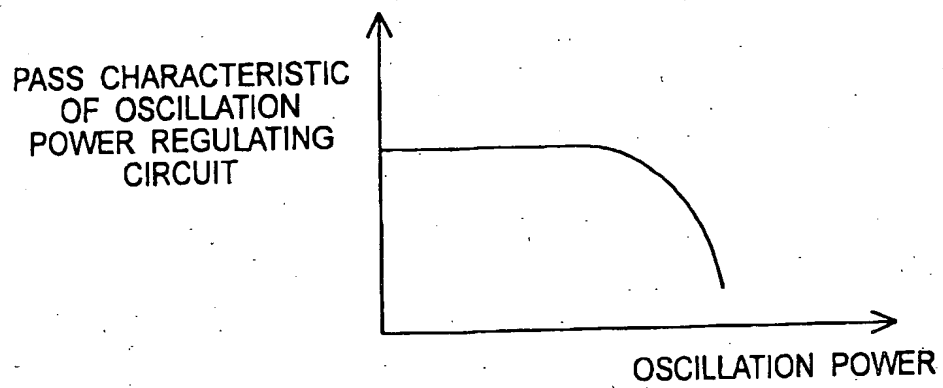


[Fig. 10]

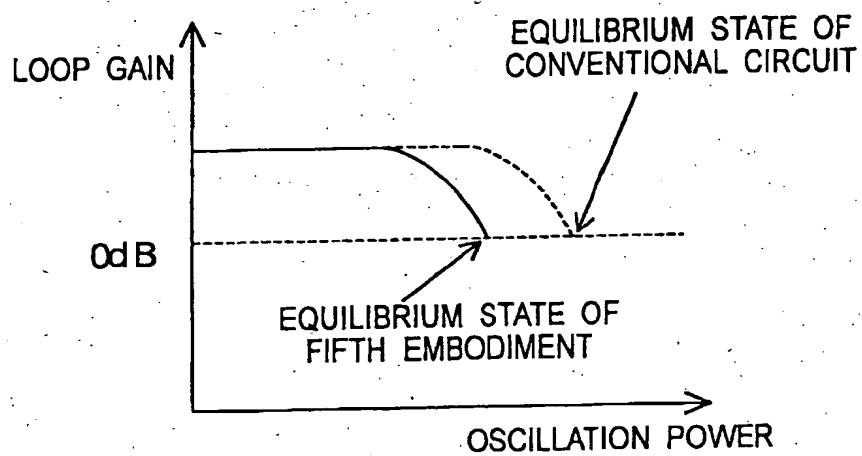


9: Amplitude power regulating circuit

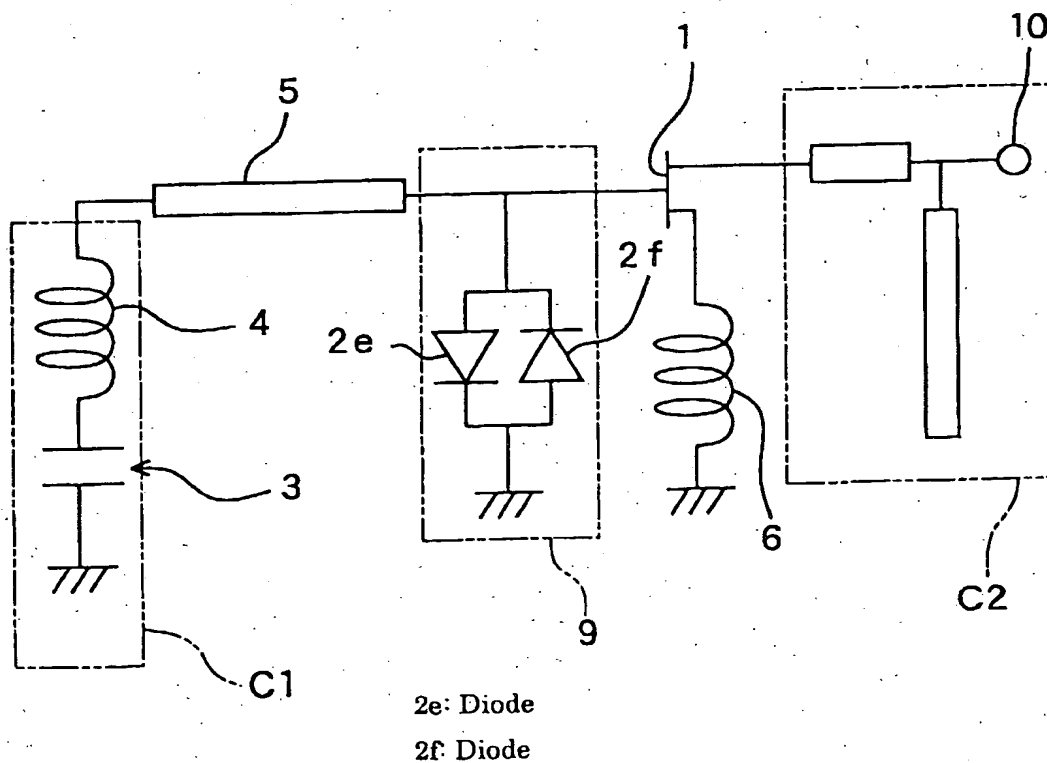
[Fig. 11]



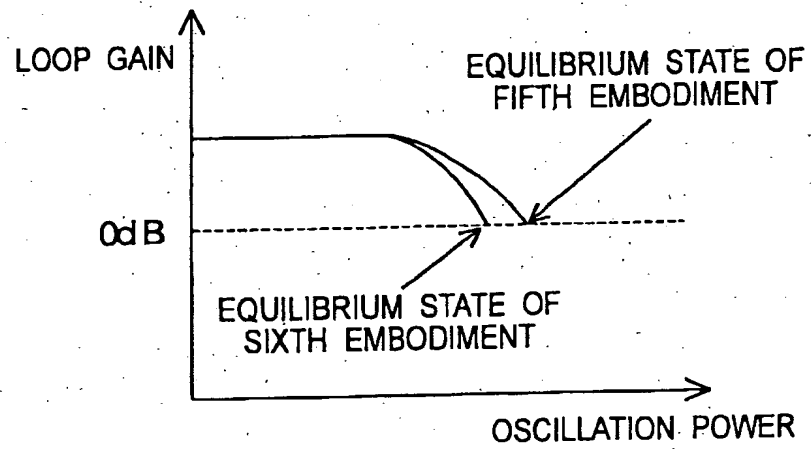
[Fig. 12]



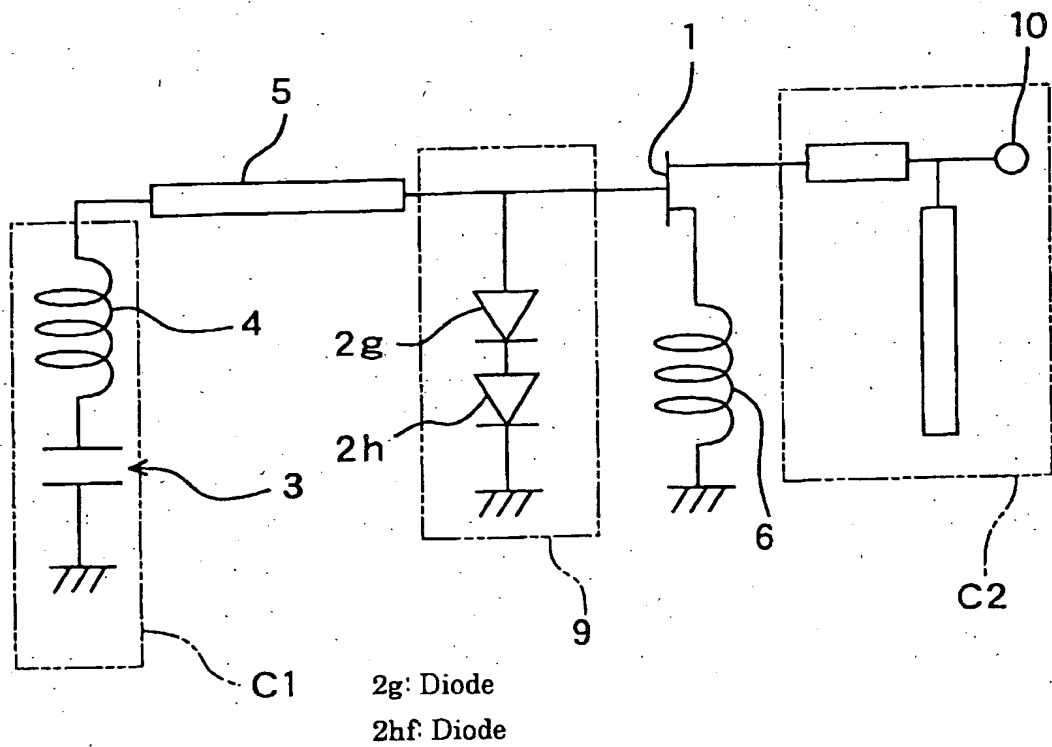
[Fig. 13]



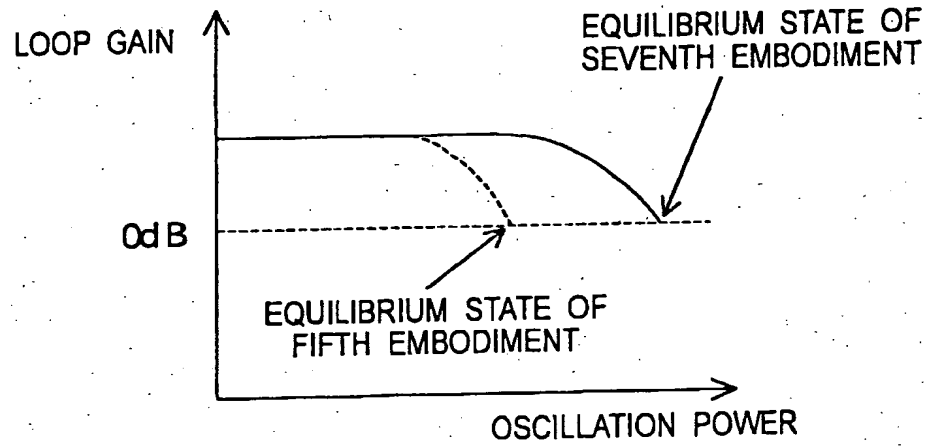
[Fig. 14]



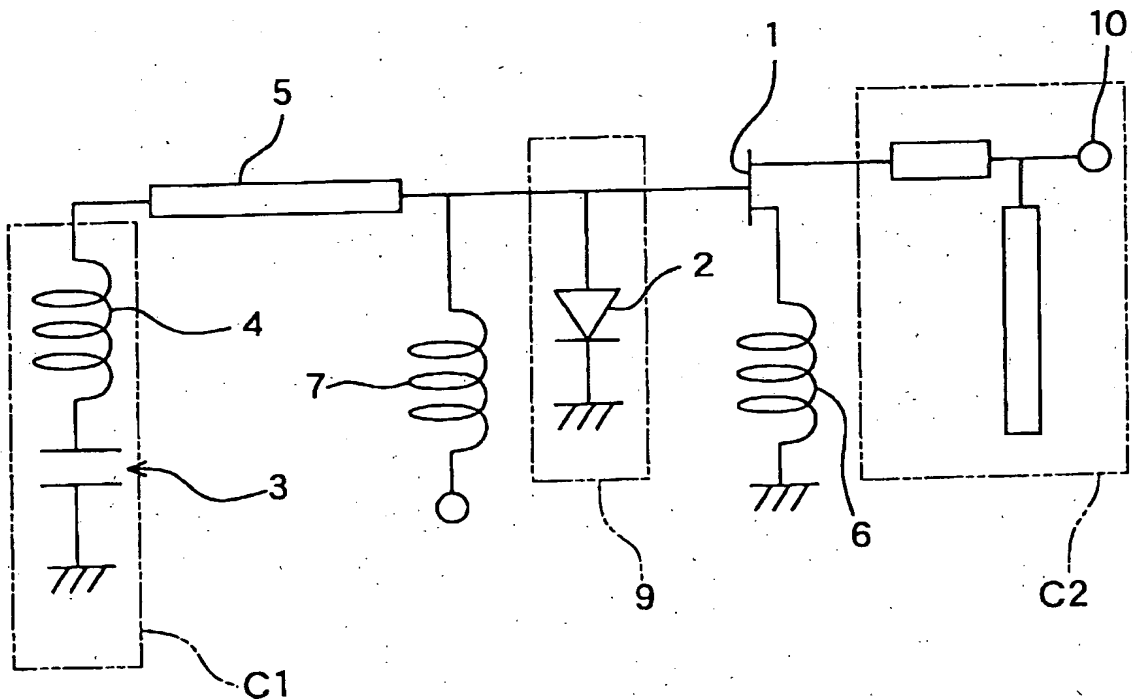
[Fig. 15]



[Fig. 16]



[Fig. 17]



[Fig. 18]

